PSEC2

Results and further testing plans

Eric Oberla

Electronics Godparent Review 10/5/2010

PSEC-2 2nd gen fast "oscilloscope on a chip"

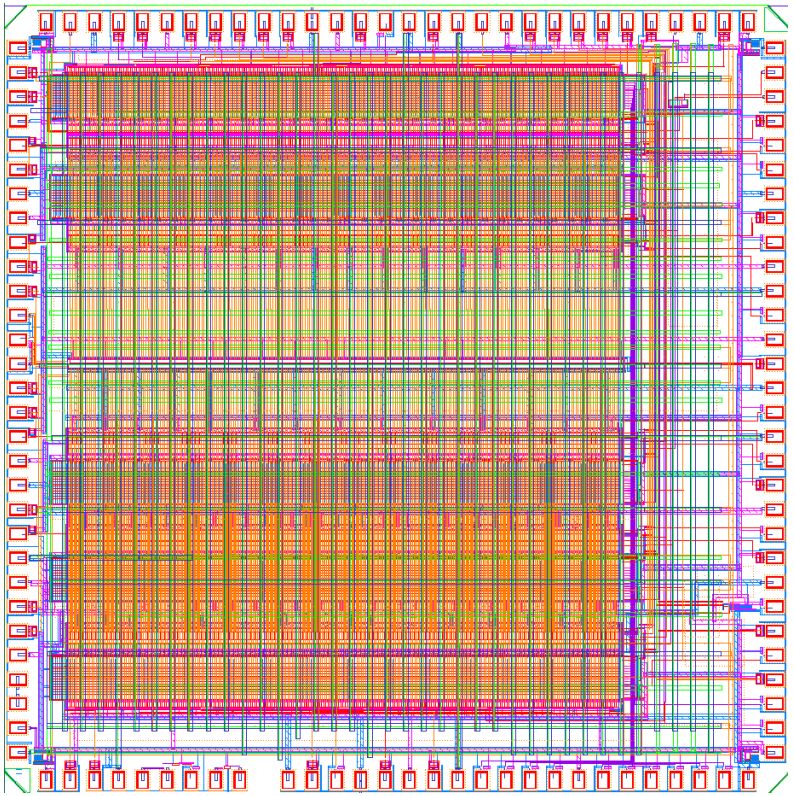
target specs

- channels: **4**
- sampling rate: **5-18 GS/s**
- sampling depth: **256**
- input bandwidth: **~ 2GHz**
- dynamic range: **1V**
- A/D conversion: **12 bits in 2 µs**
  8 bits in 130 ns
- readout: **6 µs/channel**
- power: **<100mW/channel**
- **Internal trigger**

process

- IBM 130 nm CMOS
- submitted directly to MOSIS
- chip back: June 2010

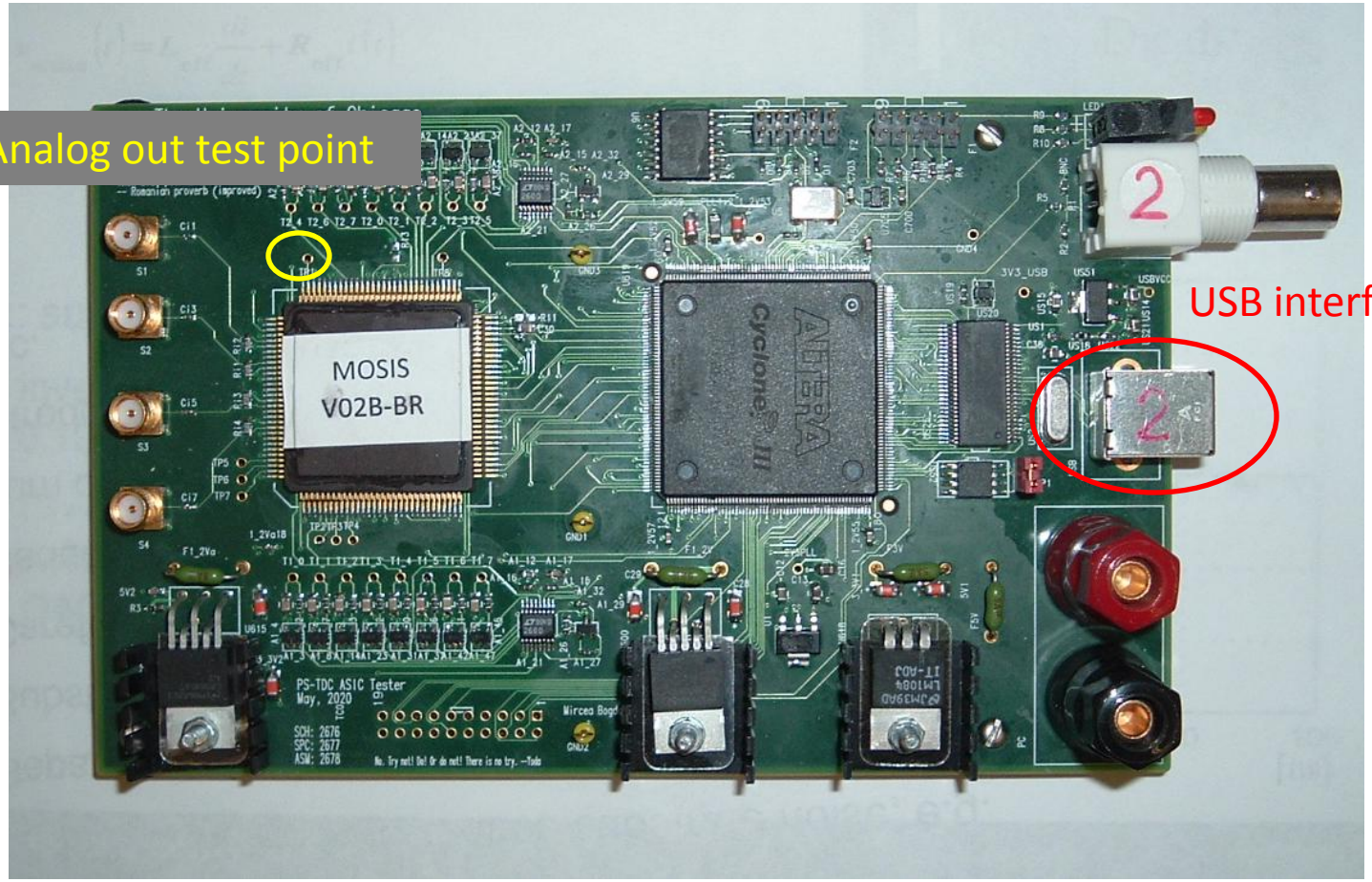
layout



area: 4.4x4.4 mm^2

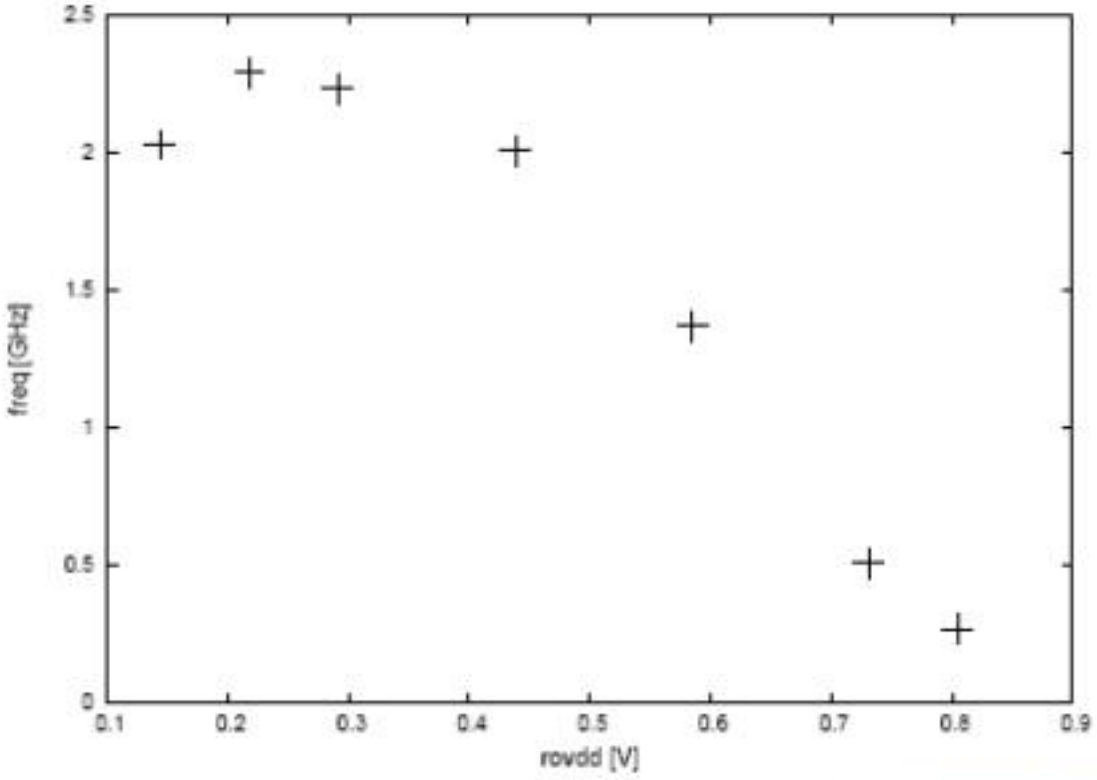
PSEC2 Eval Board

PSEC2 Eval Board

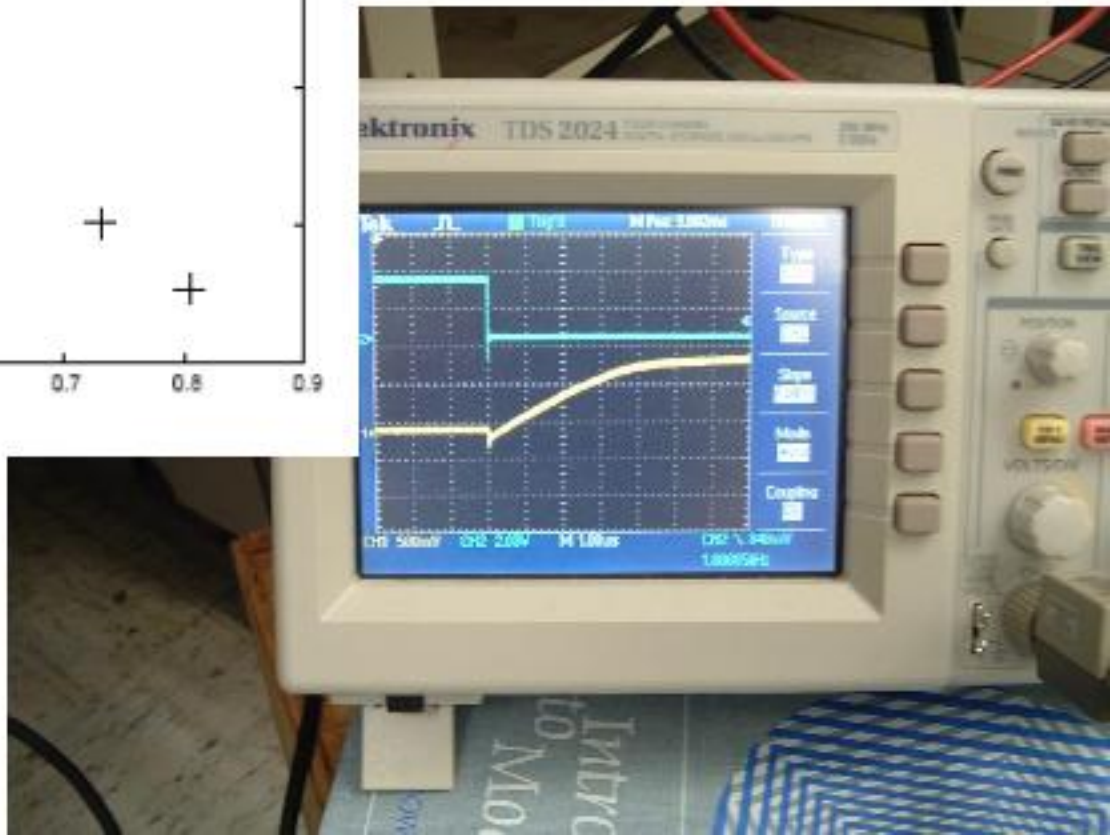


ADC Test points

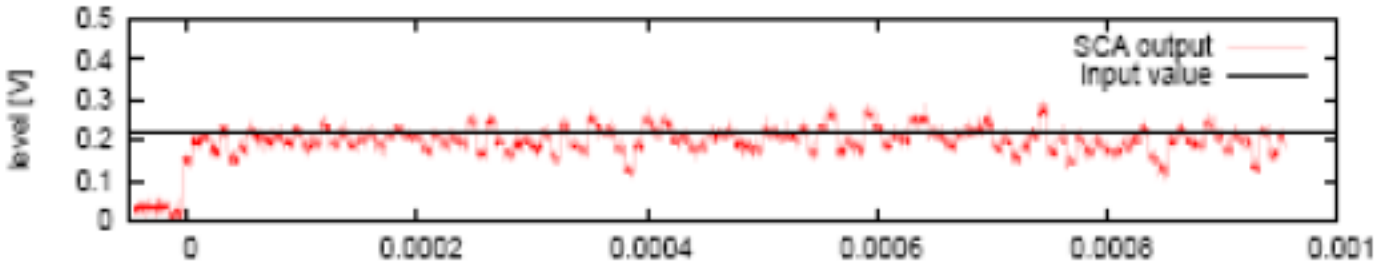
Ring Oscillator – digitization speed

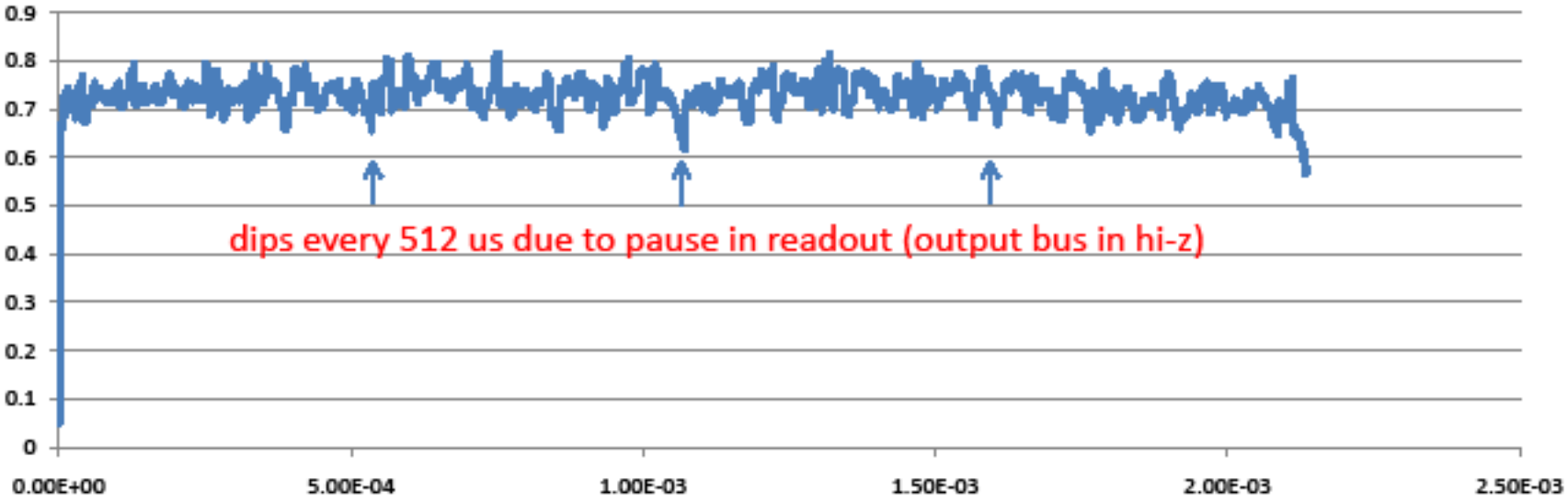


Ramp generation



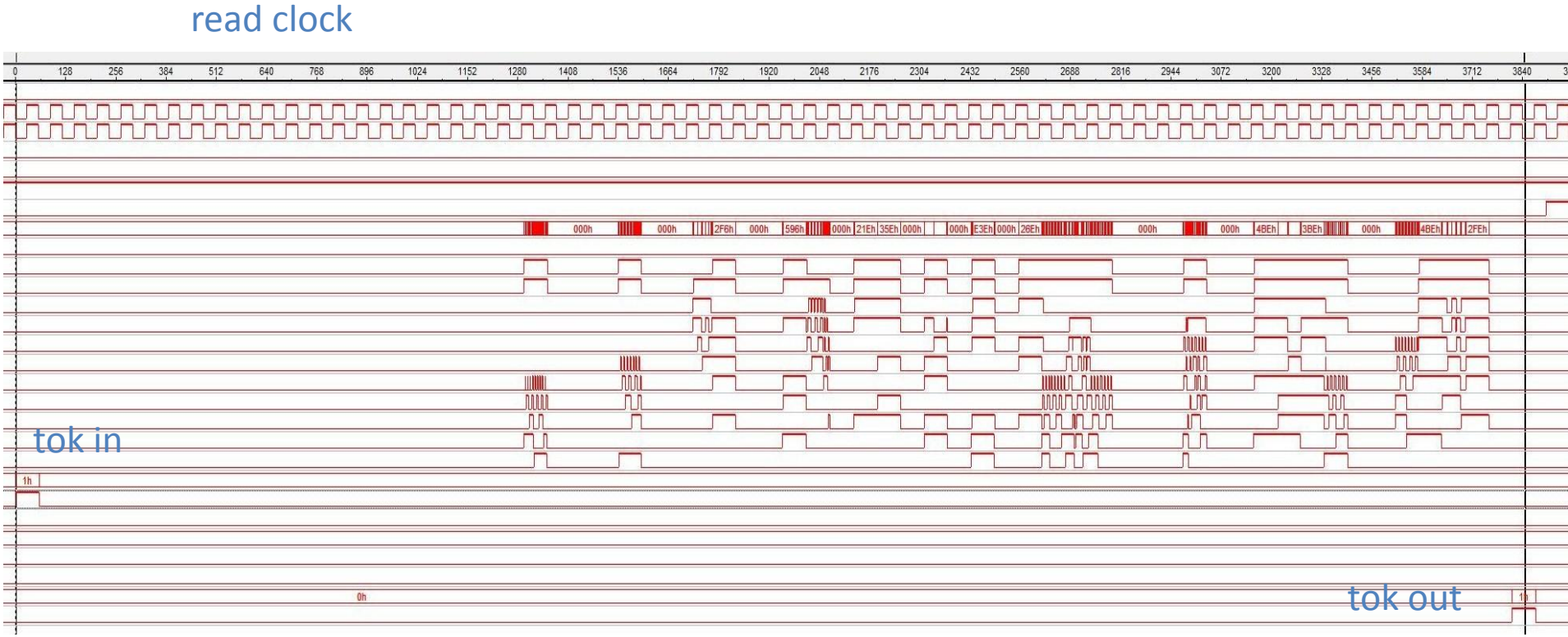
Channel 1 – Analog out (DC level)





Sampling rate: 5GS/s readout speed: 125KHz (8 us/cell)

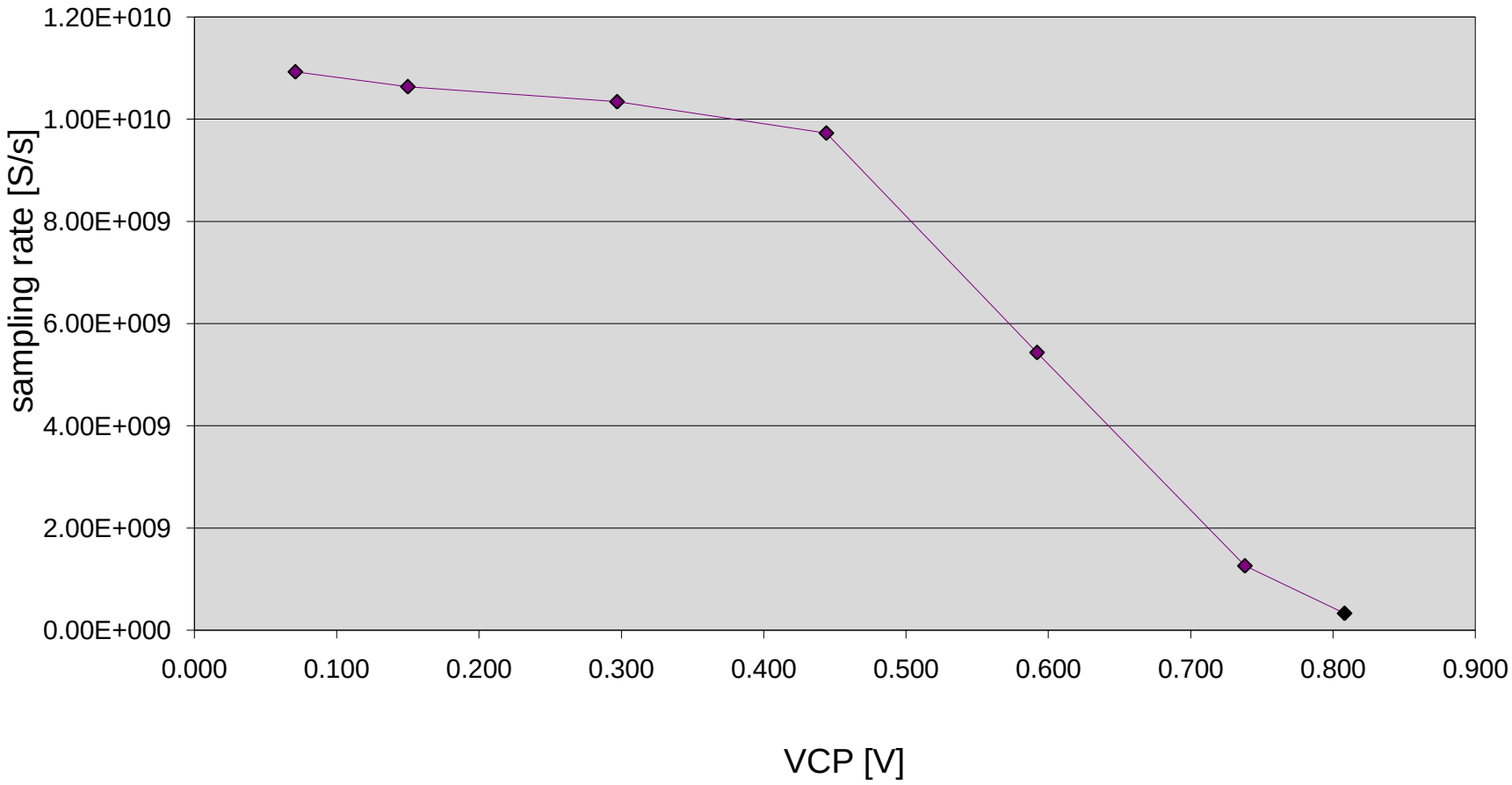
Digitization: having problems w/ Wilkinson ADC



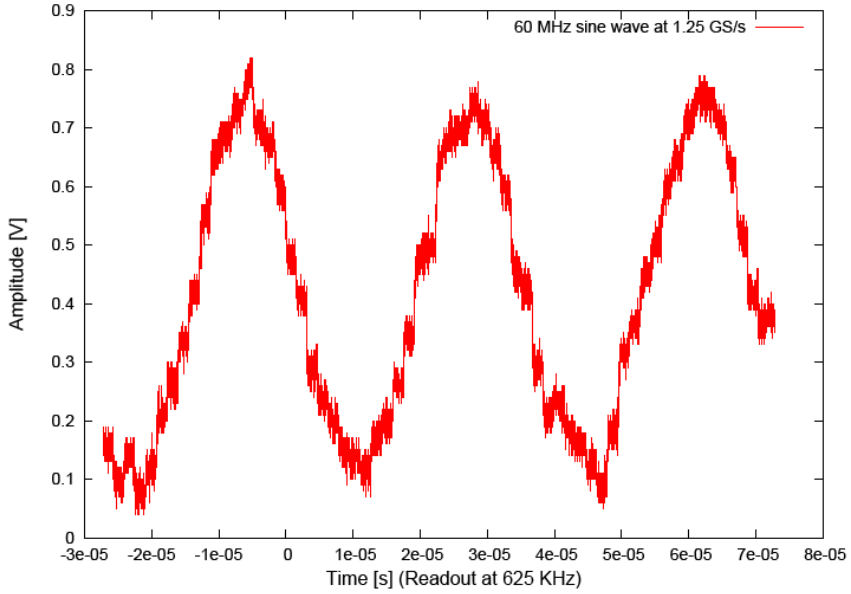
Some bits appeared to still be counting once counter is stopped – leakage developed after several microseconds of storage . Simulations confirmed that dynamic dff in ADC counters leaks.

Sampling speed measurement:

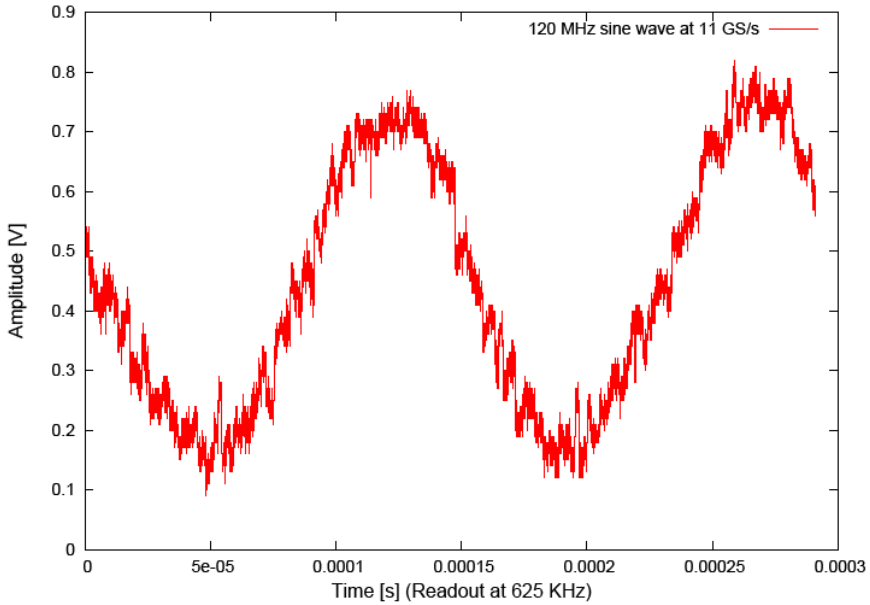
Using sine wave input to chan1, used the analog out option to measure the sampling rate (topping out ~11 GS/s)



Sampled waveforms using Analog-out



1.25 GS/s



11 GS/s

Notes: Analog values are stored on buffer input capacitance, not designated sampling capacitor. (due to error in schematic)

Noise seen here dominated by set-up (scope, probe, etc.). We are currently designing board with external ADC to better characterize the noise/bandwidth

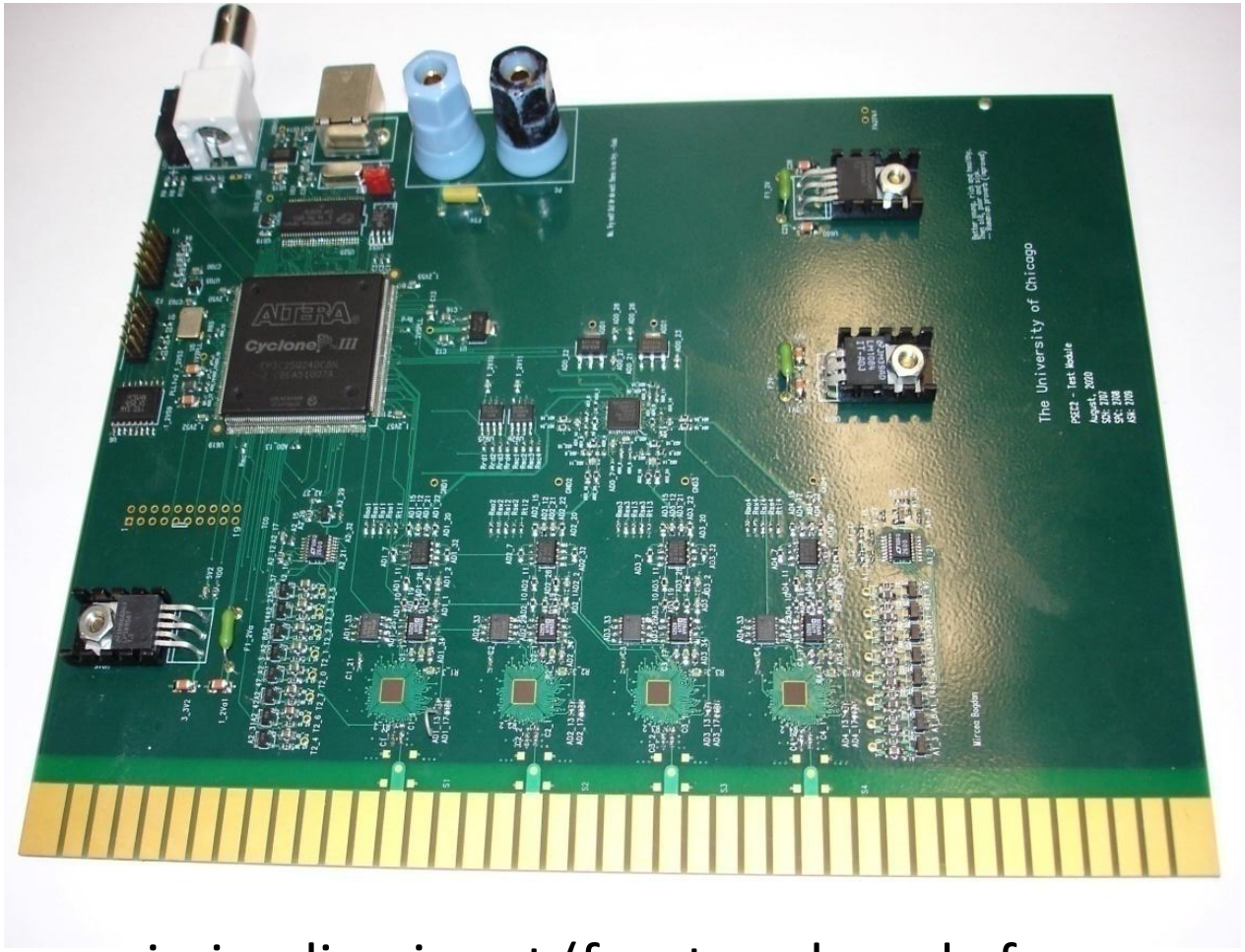
Summary

working: timing, sampling (mostly), readout, ramp
not working: A/D

Plans

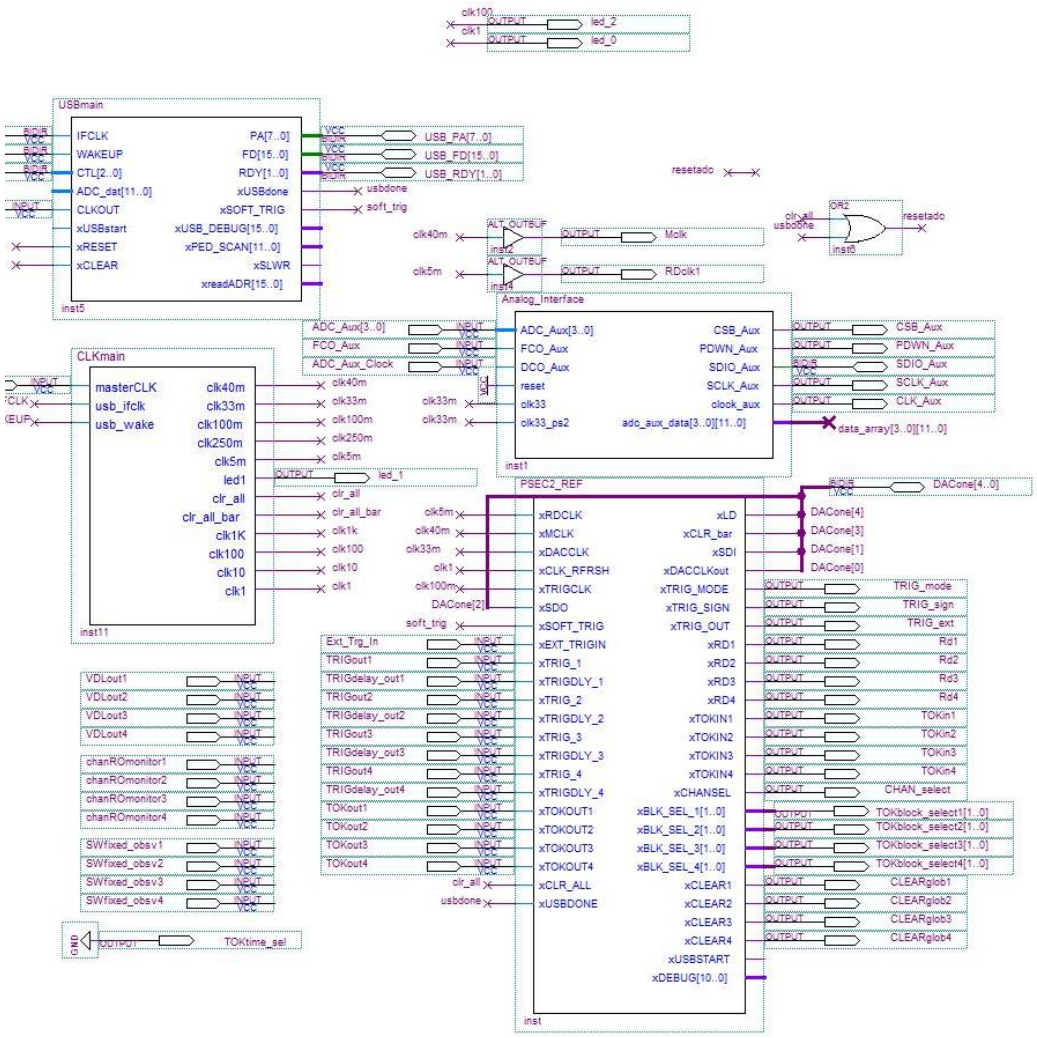
Possibly design a board with external ADC for use with Chan1 analog-out. This would allow for further chip characterization (noise and bandwidth in particular).

PSEC2 flip chip/external ADC Eval Board



Transmission line input (front-end ready for large-area MCP tray)

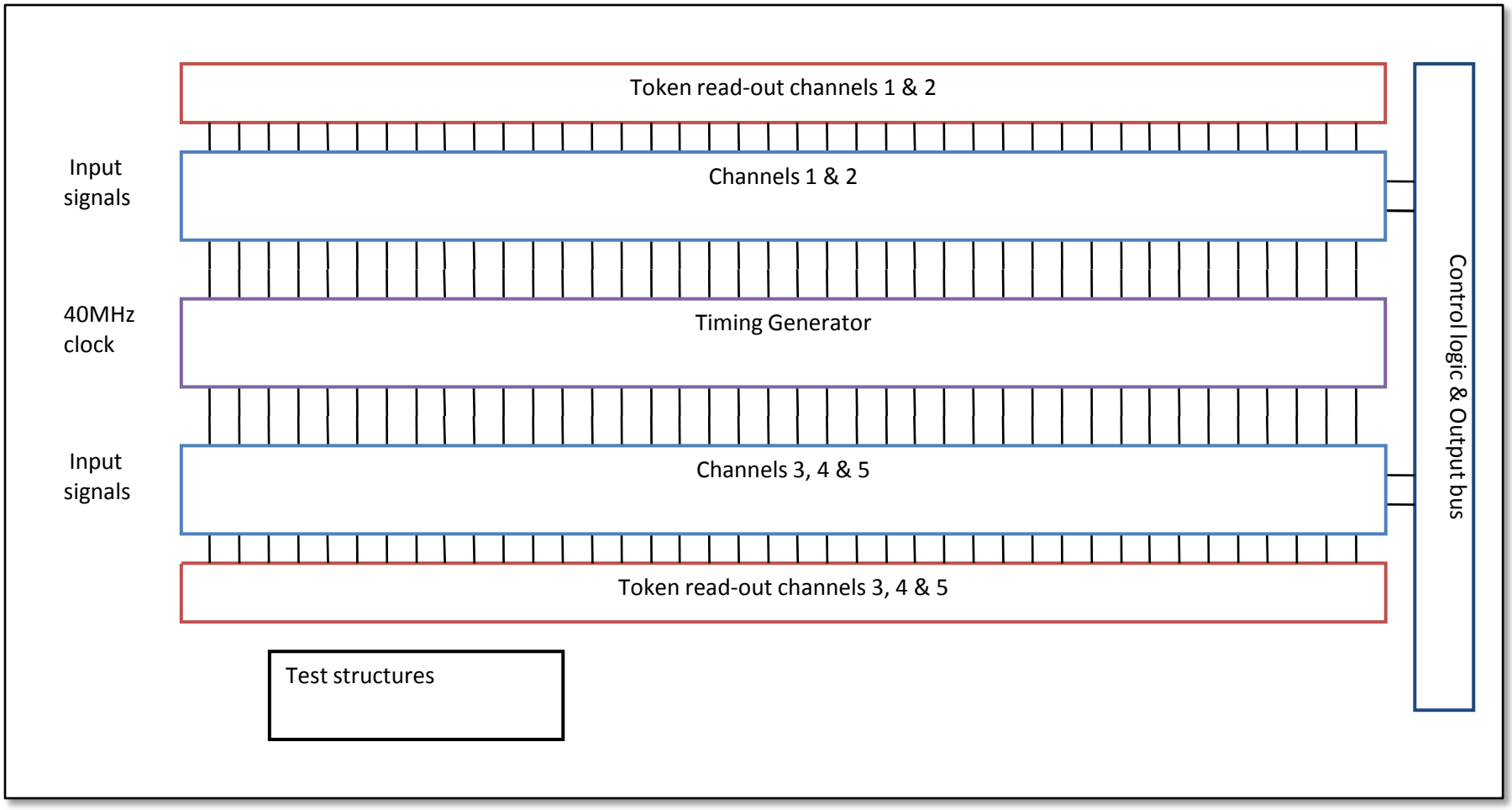
PSEC2 flip chip/external ADC Eval Board



- Firmware basically done
- board was tested in the last few days. Everything seems ok
- proceed with stud bonding of bare PSEC2s. (4x2 boards)
- Finish PSEC2 tests in next weeks…move on

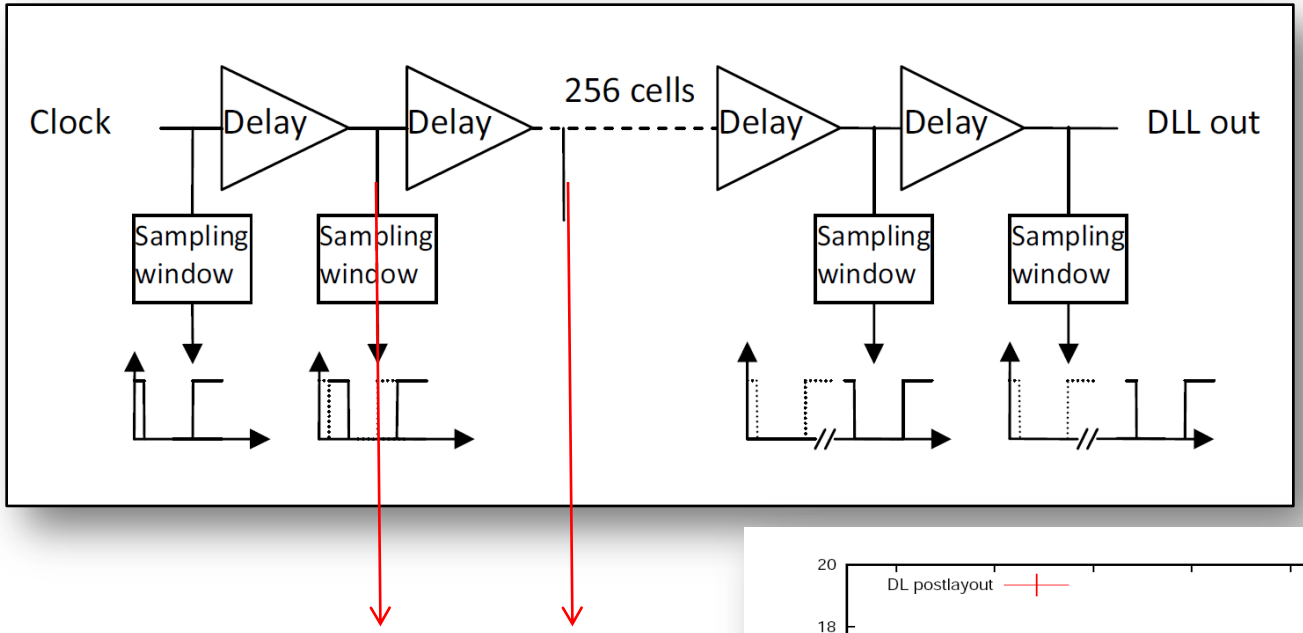
backup

Principle of Operation



block diagram

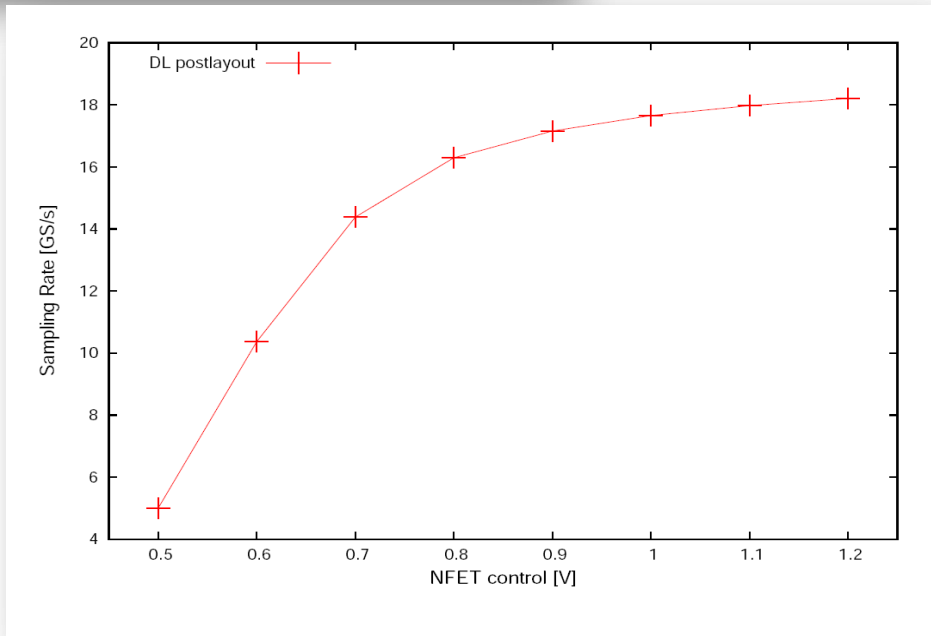
Principle of Operation - timing generator



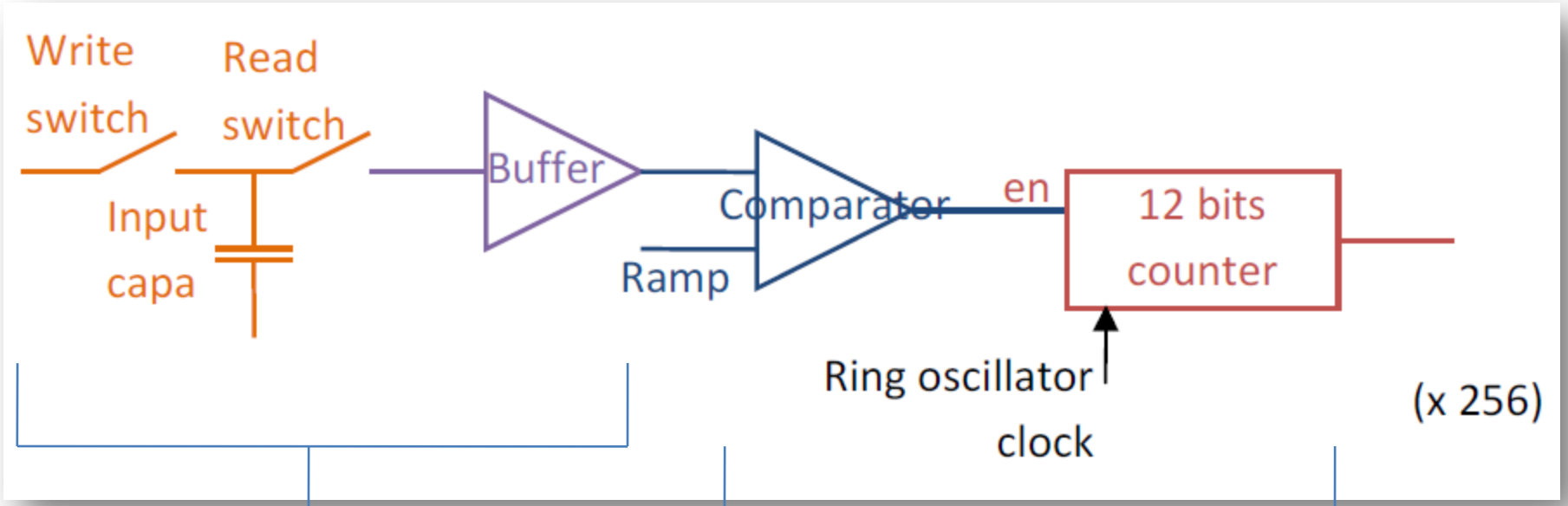
voltage-controlled delay line

delay per cell: Δt

Sampling rate = 1/ Δt



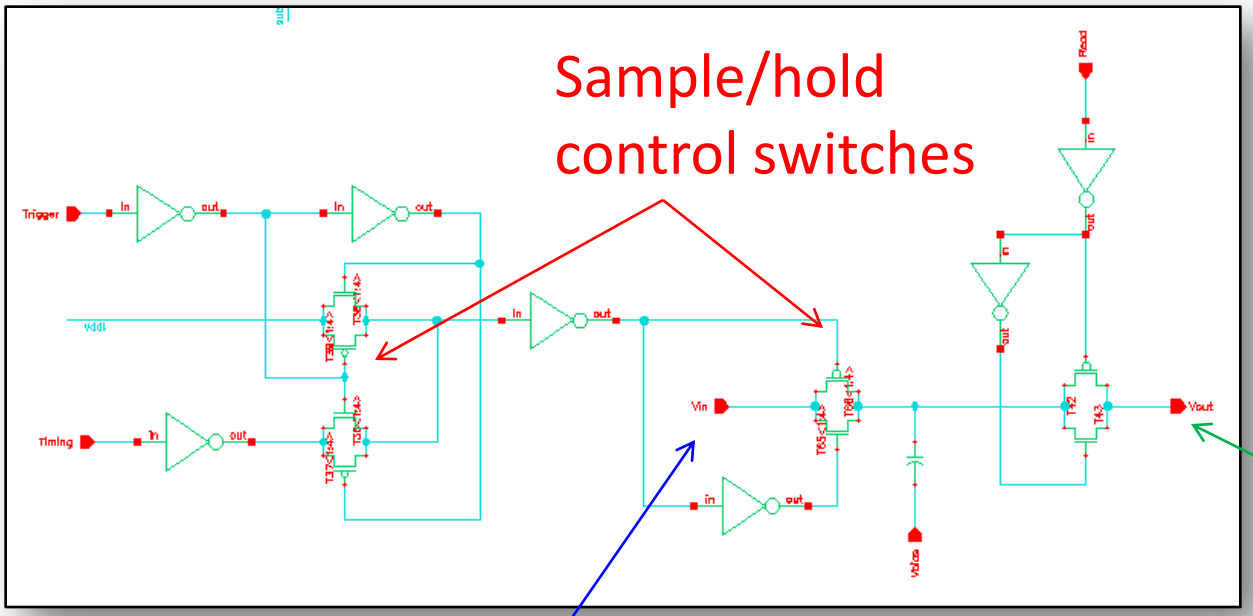
Principle of Operation – channel block diagram



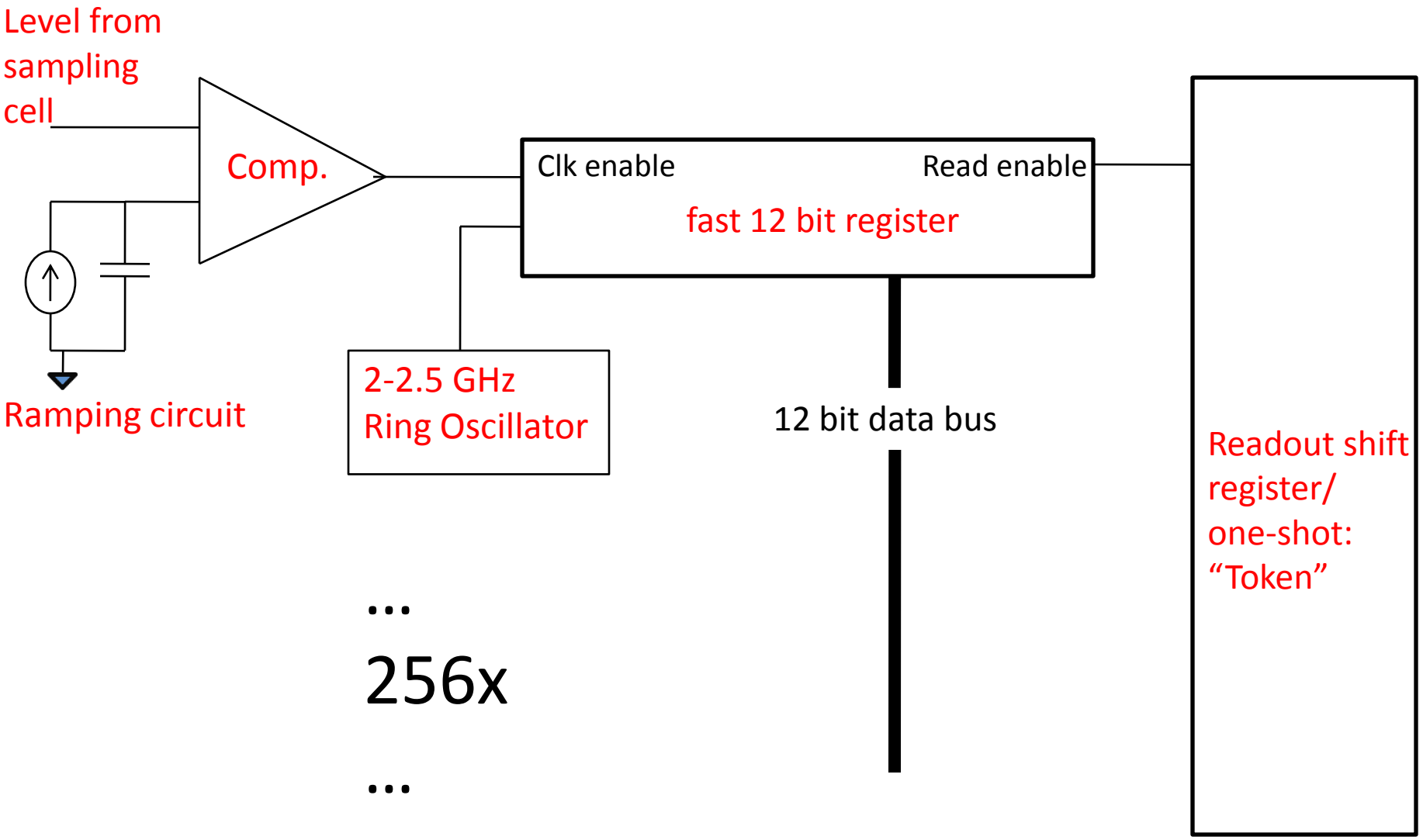
switched capacitor array

Wilkinson ADC

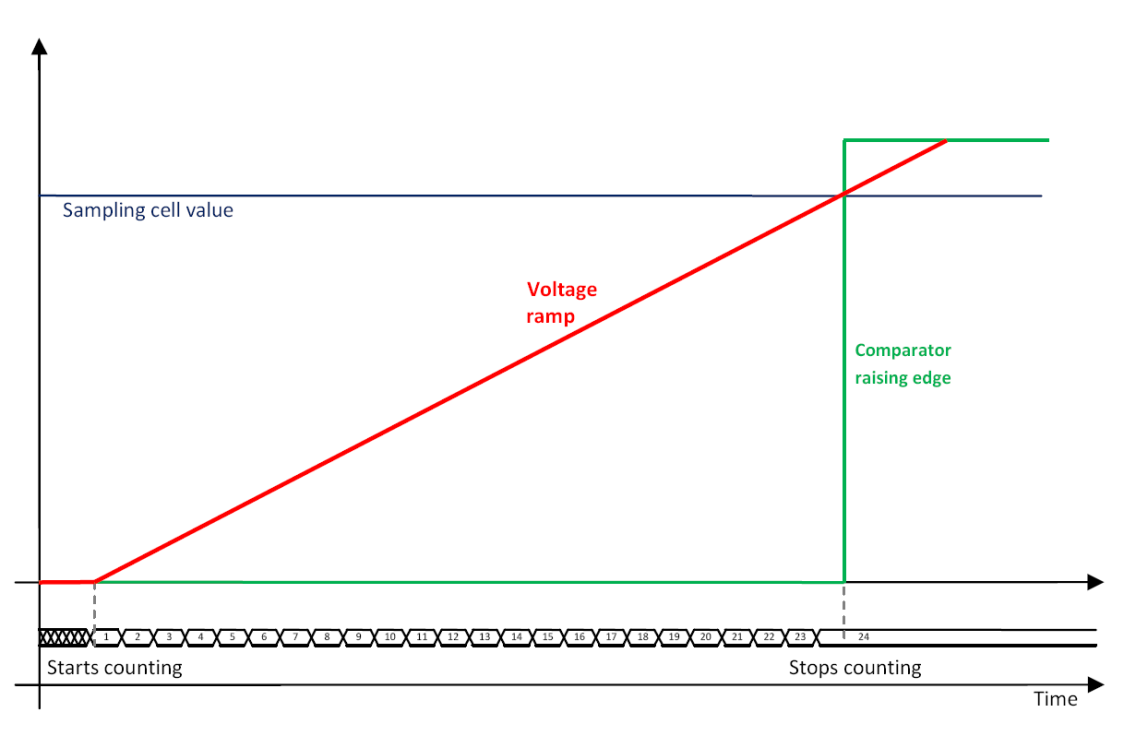
Principle of Operation – switched cap circuit



Principle of Operation – ADC & Readout



Principle of Operation – ADC & Readout



A/D conversion ↑

Token readout →